REMARKS

Claims 47-59 are pending in the application with claims 47, 48, and 52 amended herein and new claims 55-59 added herein.

Claim 47 is objected to because of informalities in claim terminology that are revised herein by amendment as requested. Applicants request withdrawal of the objection.

Claims 47-53 stand rejected under 35 USC 102(e) as being anticipated by Fukada. Applicants request reconsideration.

Amended claim 47 sets forth an integrated circuit that includes, among other features, a layer containing a first metal over a semiconductive substrate and a layer of alloy material within the layer containing the first metal, the alloy material containing the first metal and a second metal different from the first metal. The second metal contains palladium, magnesium, or both. The integrated circuit also includes a conductive connection on the alloy layer. Pages 2-3 of the Office Action allege that Fukada discloses the integrated circuit of claim 47. However, Fukada does not disclose or suggest the alloy material of claim 47. Specifically, Fukada does not provide any teaching of palladium, magnesium, or both in combination with a first metal forming a layer of alloy material within a layer of the first metal. Anticipation requires disclosure of each and every element. At least for such reasons Fukada does not anticipate claim 47.

Claims 48-53 depend from claim 47 and are thus not anticipated at least for such reason as well as the additional limitations of such claims not disclosed or suggested. For example, amended claim 48 sets forth that the alloy material consists of an intermetallic. Fukada does not disclose or suggest an intermetallic. Also for example, amended claim

52 sets forth that the second metal comprises palladium. Fukada does not provide any mention of palladium. Accordingly, Applicants request allowance of claims 47-53 in the next Office Action.

Claims 47-54 stand rejected under 35 USC 103(a) as being unpatentable over You in view of Aoyama. Applicants request reconsideration.

The subject matter of claim 47 is described above. Pages 3-4 of the Office Action allege that You discloses the integrated circuit of claim 47 except for a conductive connection formed on the alloy layer and relies on Aoyama for such a teaching. However, neither You nor Aoyama disclose or suggest a layer of alloy material within a layer containing a first metal, the alloy material containing the first metal and a second metal different from the first metal wherein the second metal includes palladium, magnesium, or both. Review of You and Aoyama reveals that neither reference discloses nor suggests a layer of alloy material including palladium, magnesium, or both. Since both references are deficient in the same respects, a combination of the references cannot somehow be considered to disclose or suggest the missing feature. At least for such reason, claim 47 is patentable over You in view of Aoyama.

Claims 48-54 depend from claim 47 and are further patentable at least for such reason as well as the additional limitations of such claims not disclosed or suggested. For example, amended claim 52 sets forth that the second metal comprises palladium. Neither You nor Aoyama provide any mention of palladium. Accordingly, Applicants request allowance of claims 47-54 in the next Office Action.

New claim 55 sets forth an integrated circuit that includes, among other features, a layer containing copper over a semiconductive substrate and a layer of alloy material within the layer containing copper, the alloy material containing intermetallic Cu_3Ti. The integrated circuit also includes a conductive connection on the alloy layer. Page 9, line 21 to page 10, line 2 and elsewhere throughout the present specification support the subject matter of claim 55. Notably, Cu_3Ti advantageously exhibits approximately the same resistivity as copper and may be useful in forming the claimed conductive connection on the alloy layer. Review of the cited references reveals that none of the references disclose or suggest intermetallic Cu_3Ti. You merely describes $CuTi_2$. You does not provide a teaching of any method that necessarily produces intermetallic Cu_3Ti. You does not appear to contemplate either a thickness of titanium layer 14 or anneal temperatures and times sufficient to produce Cu_3Ti in preference to $CuTi_2$. You further does not provide any motivation to modify the teachings therein in a manner that would produce the integrated circuit of claim 55. Claims 56-58 depend from claim 55 and are further patentable at least for such reason as well as the additional limitations of such claims not disclosed or suggested.

New claim 59 sets forth an integrated circuit that includes, among other features, a layer consisting of copper over a semiconductive substrate and a layer of alloy material within the copper layer, the alloy material layer consisting of copper along with palladium, magnesium, or both. A conductive connection is formed on the alloy layer. As discussed above regarding claim 47, all of the cited references fail to disclose or suggest palladium, magnesium, or both. Accordingly, claim 59 is patentable over the cited references.

Applicants herein set forth adequate reasons for allowance of claims 47-54 over the cited references as well as new claims 55-59. Applicants request allowance of all of pending claims 47-59 in the next Office Action.

Respectfully submitted,

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Filing Date ..... June 13, 2001
Inventor ..... Dinesh Chopra, et al
Assignee..... Micron Technology, Inc.
Group Art Unit 2814
Examiner ..... P. Cao
Attorney's Docket No. MI22-1747
Title: Conductive Connection Forming Methods, Oxidation Reducing Methods, and Integrated Circuits Formed Thereby

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO JANUARY 3, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

47. (amended) An integrated circuit comprising:

a semiconductive substrate;

a layer comprising a first metal over the substrate;

a layer of alloy material within the layer comprising the first metal ~~comprising layer~~, the alloy material layer comprising the first metal and a second metal different from the first metal, the second metal comprising palladium, magnesium, or both; and

a conductive connection on the alloy layer.

48. (amended) The integrated circuit of claim 47 wherein the alloy material consists ~~essentially~~ of an intermetallic.

52. (amended) The integrated circuit of claim 47 wherein the second metal comprises ~~aluminum, titanium,~~ palladium~~, magnesium, or two or more such metals~~.

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